Laboratory 2

(Due date: **002**: February 8th, **003**: February 9th)

OBJECTIVES

- ✓ Use the Concurrent Description and the Structural Description in VHDL.
- ✓ Implement Combinational circuits on an FPGA.

VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

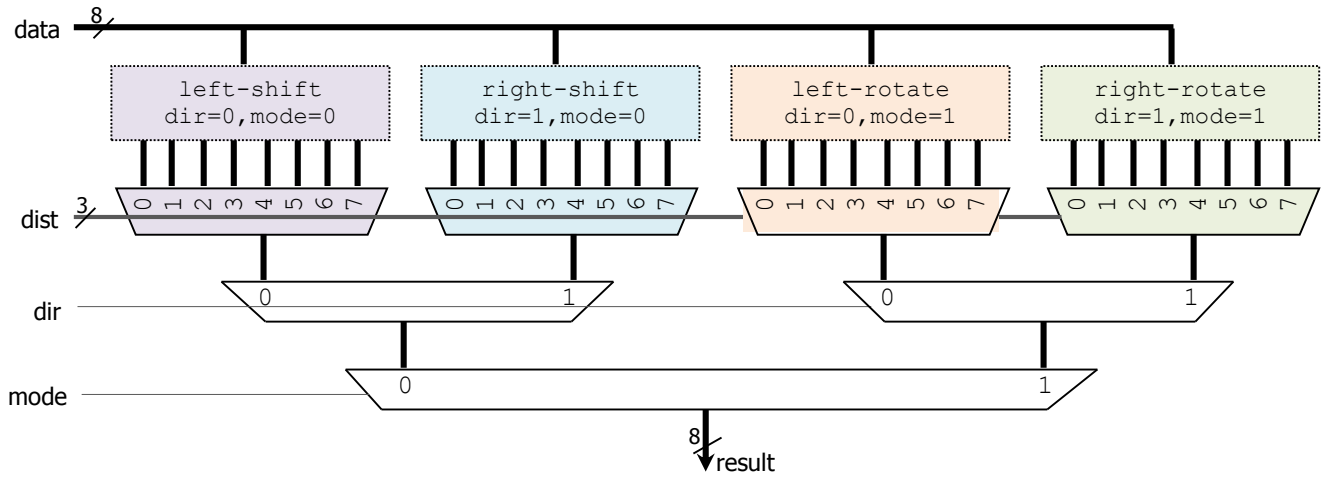
FIRST ACTIVITY: (100/100)

- **8-BIT BARREL SHIFTER:** This circuit transforms an 8-bit input into an 8-bit output, based on the inputs `dist[2..0]`, `dir`, and `mode`, which specify several shifting/rotation options.

- **Operation**:
  - ✓ `result[7..0]`: It is shifted version of the input `data[7..0]`.
  - ✓ `mode`: It controls the operation mode.
    - `mode=0` (arithmetic mode): when shifting to the right, sign-extension is used. Shifting to the left inserts 0's.
    - `mode=1` (rotation mode): when shifting to the right or left, no bits are lost (they wrap-around).
  - ✓ `dir`: It controls the shifting direction (`dir=1`: to the right, `dir=0`: to the left).
  - ✓ `dist[2..0]`: number of bits to shift.

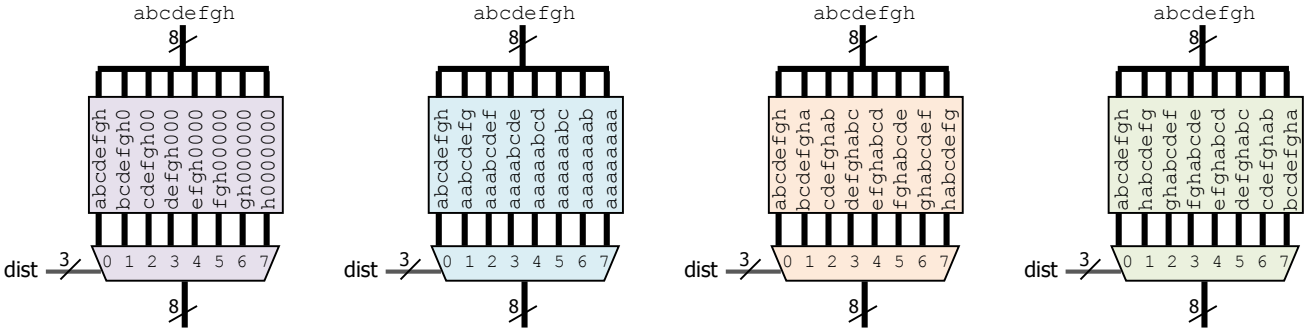
- The circuit consists of four 8-to-1 bus muxes (8 bits) and three 2-to-1 bus muxes (3 bits) that are interconnected together. The inputs to the 8-to-1 bus muxes are rearranged versions of the 8-bit input: `abcdefgh`.

mode = 0. ARITHMETIC MODE				mode = 1. ROTATION MODE			
dir	dist[2..0]	data[7..0]	result[7..0]	dir	dist[2..0]	data[7..0]	result[7..0]
0	0 0 0	abcdefgh	abcdefgh	0	0 0 0	abcdefgh	abcdefgh
0	0 0 1	abcdefgh	bcdefgh0	0	0 0 1	abcdefgh	bcdefgha
0	0 1 0	abcdefgh	cdefgh00	0	0 1 0	abcdefgh	cdefghab
0	0 1 1	abcdefgh	defgh000	0	0 1 1	abcdefgh	defghabc
0	1 0 0	abcdefgh	efgh0000	0	1 0 0	abcdefgh	efghabcd
0	1 0 1	abcdefgh	fgh00000	0	1 0 1	abcdefgh	fghabcde
0	1 1 0	abcdefgh	gh000000	0	1 1 0	abcdefgh	ghabcdef
0	1 1 1	abcdefgh	h0000000	0	1 1 1	abcdefgh	habcdefg
1	0 0 0	abcdefgh	abcdefgh	1	0 0 0	abcdefgh	abcdefgh
1	0 0 1	abcdefgh	aabcdefg	1	0 0 1	abcdefgh	habcdefg
1	0 1 0	abcdefgh	aaabcdef	1	0 1 0	abcdefgh	ghabcdef
1	0 1 1	abcdefgh	aaaabcde	1	0 1 1	abcdefgh	fghabcde
1	1 0 0	abcdefgh	aaaaabcd	1	1 0 0	abcdefgh	efghabcd
1	1 0 1	abcdefgh	aaaaaabc	1	1 0 1	abcdefgh	defghabc
1	1 1 0	abcdefgh	aaaaaaab	1	1 1 0	abcdefgh	cdefghab
1	1 1 1	abcdefgh	aaaaaaaa	1	1 1 1	abcdefgh	bcdefgha



Instructor: Daniel Llamocca
TAs: Michael Lohrer, Jing Wu

- The following figure specifies the exact inputs to each 8-to-1 bus mux:



- **VIVADO DESIGN FLOW FOR FPGAS:**
  - ✓ Create a new Vivado Project. Select the **XC7A100T-1CSG324 Artix-7 FPGA** device.
  - ✓ Write the VHDL code for the barrel shifter.
    - To implement the 2-to-1 bus mux and the four 8-to-1 bus muxes (each with different inputs), it is strongly advised that you use the VHDL concurrent statements.
    - To implement the top file, use the Structural Description: Create a separate file for the 2-to-1 bus mux, for each 8-to-1 bus mux, and the top file (where you will interconnect all the components).
  - ✓ Write the VHDL testbench to test the circuit for all possible variations of `dist`, `dir`, and `mode`. For `data` use: `10101101` and `01110011`. In total, you should text 64 cases.
  - ✓ Perform Functional Simulation. **Demonstrate this to your TA**.
  - ✓ I/O Assignment: Create the XDC file.
    Nexys-4 DDR Board: Use `SW7-SW0` for `data[7..0]`, `SW10-SW8` for `dist[2..0]`, `SW11` for `dir`, and `SW12` for `mode`. Use `LED7-LED0` for `result[7..0]`.
  - ✓ Perform Timing Simulation. **Demonstrate this to your TA**.
  - ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA**.

- Submit (as a .zip file) all the generated files: VHDL code files, VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____ **Date:** _____